CLAIMS

We claim:

1. A sense amplifier circuit comprising:

a sense amplifier coupled to a first input line and a second input line and adapted to receive an enable signal, wherein the enable signal controls whether the sense amplifier is enabled;

a first inverter coupled to the first input line and adapted to provide a first output signal;

a second inverter coupled to the second input line and adapted to provide a second output signal; and

a logic gate adapted to receive the first output signal and the second output signal and to provide a trip signal.

2. The sense amplifier circuit of Claim 1, wherein the trip signal indicates when the sense amplifier has read a data value provided on the first input line and/or the second input line and when the first input line and the second input line are precharged.

3. The sense amplifier circuit of Claim 1, further comprising a latch adapted to store a result provided by the first output signal or the second output signal, wherein the result is stored by the latch when the trip signal transitions to a first value.

4. The sense amplifier circuit of Claim 1, further comprising:

a latch adapted to store a result provided by the first output signal or the second output signal, wherein the result is stored by the latch when the trip signal transitions to a first value; and

a precharge circuit adapted to precharge the first input line and/or the second input line, wherein when the enable signal enables the sense amplifier, the precharge circuit stops precharging the first input line and/or the second input line.

5. The sense amplifier circuit of Claim 1, further comprising:

a latch adapted to store a result provided by the first output signal or the second output signal, wherein the result is stored by the latch when the trip signal transitions to a first value;

a precharge circuit adapted to precharge the first input line and/or the second input line when the enable signal transitions to a first value, with the trip signal transitioning to a second value when the first input line and/or the second input line reach precharge values; and

a column multiplexer adapted to select which data lines to couple to the first input line and/or the second input line, wherein when the enable signal enables the sense amplifier by transitioning to a second value, the precharge circuit stops precharging the first input line and/or the second input line and the column multiplexer couples at least one data line to the first input line and/or the second input line.

6. The sense amplifier circuit of Claim 5, further comprising a global precharge circuit adapted to precharge the data lines.

7. The sense amplifier circuit of Claim 1, further comprising a sense amplifier circuit controller adapted to control one or more of the sense amplifier circuits by controlling the enable signal and monitoring the trip signal of each of the sense amplifier circuits.

8. The sense amplifier circuit of Claim 1, wherein the first and second input lines are couplable to bitlines of a memory array, wherein the memory array comprises a number of sense amplifier circuits adapted to read data stored in the memory array.

9. A memory array comprising:

a plurality of sense amplifiers adapted to read data provided on bitlines;

a plurality of corresponding precharge circuits adapted to precharge the bitlines coupled to the sense amplifiers;

a plurality of corresponding inverters coupled to the bitlines and adapted to provide output signals based on signal levels on the bitlines coupled to the sense amplifiers;

a plurality of corresponding logic gates adapted to receive the output signals from the corresponding inverters and to provide trip signals based on the output signals; and

a plurality of corresponding latches adapted to store the output signals from one of the corresponding inverters under control of the corresponding trip signals, wherein the trip signals transition to a first value when the corresponding bitlines are precharged and transition to a second value when the corresponding sense amplifiers read the data on the corresponding bitlines.

10. The memory array of Claim 9, wherein the sense amplifiers are disabled when the corresponding trip signals transition to the second value.

11. The memory array of Claim 9, wherein the precharge circuits are enabled to precharge the corresponding bitlines when the corresponding trip signals transition to the second value.

12. The memory array of Claim 9, further comprising a plurality of sense amplifier controllers with each associated with one or more of the sense amplifiers, wherein the sense amplifier controllers control the enabling and disabling of the associated sense amplifiers and the associated precharge circuits based on the associated trip signals.

13. The memory array of Claim 12, further comprising a plurality of column multiplexers adapted to couple selected data lines to the bitlines of the corresponding sense amplifiers, wherein the column multiplexers are enabled by the associated sense amplifier controllers.

14. A method of reading data from data lines, the method comprising:

disabling a sense amplifier coupled to the data lines;

precharging the data lines;

providing a first signal value via inverters coupled to the data lines when the data lines are precharged;

providing the data on the data lines after the first signal value is provided;

enabling the sense amplifier to read the data placed on the data lines after the first signal value is provided; and

providing a second signal value via the inverters coupled to the data lines when the sense amplifier has read the data placed on the data lines.

15. The method of Claim 14, further comprising repeating the method by disabling the sense amplifier and precharging the data lines after the second signal value is provided.

16. The method of Claim 14, further comprising storing an output signal provided by one of the inverters when the second signal value is provided.

17. The method of Claim 14, further comprising disabling the precharging after the first signal value is provided.